Maximize Your AI Compatibility with Flexible Pre- and Post-Processing

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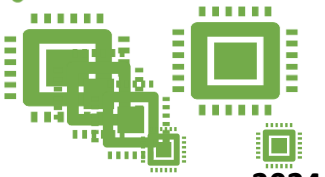
Flex Logix

flexlogix
reconfigurable

Changing Economics → Chips Need to Evolve & Adapt

Skyrocketing Fab Costs

IC tapeout costs increasing significantly



Decreasing IC Selection

Forcing IC manufacturers to reduce # of chips/family, especially impacting smaller ICs

Increasing Complexity

All while design complexity increases and emerging technologies continually evolve

Adaptability Required

That provide reprogrammable algorithm acceleration that meets SWaP Goals

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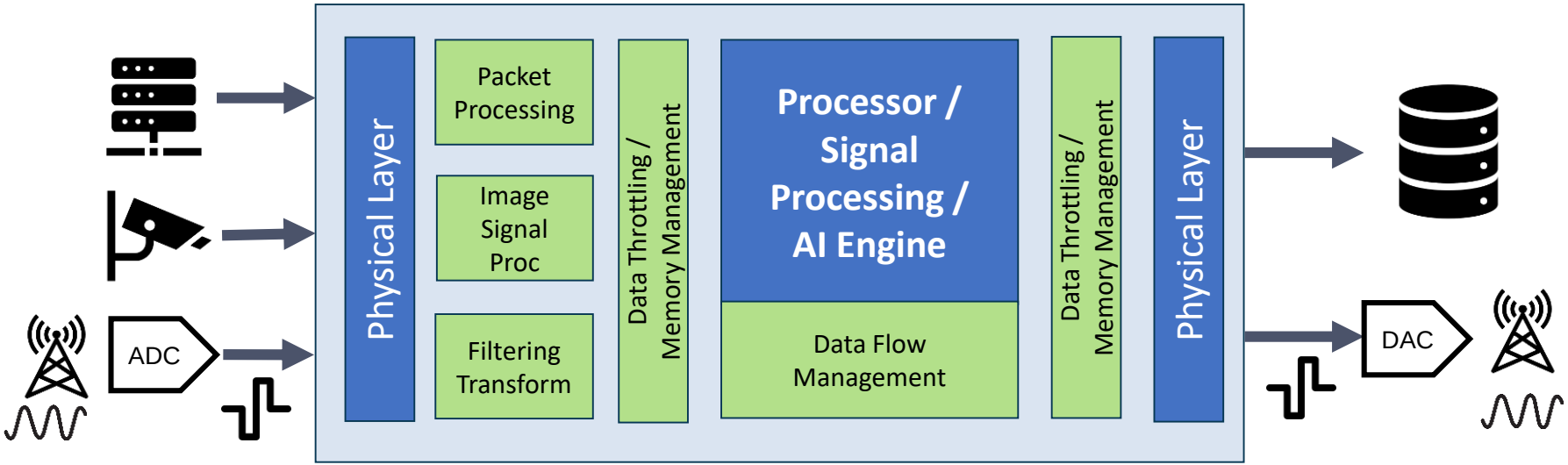
eFPGA Complements AI and Signal Processing

eFPGA Enables Greater Market Applicability and Differentiation

Data sources vary and require different preprocessing

Data requires management, formatting, throttling

For export, data needs to be packetized and buffered



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Dynamic Nature of Data & Algorithms

Changing Protocols

- Interfaces Specific Protocols
- Distinct Applications Demands
- Unique Regional Requirements

1G → 100G+

IPv4 → HTTP/2

USA vs EU

Evolving Algorithms

- Inferencing Algorithms
- Adaptive Filtering / Kalman
- Compression Solutions

YOLO v1 → v5

Scalar → Vector

LZW → Dictionary

Emerging Threats

- Evolving Threats / Aging Cryptography
- Digital Signing / Authentication
- PQC Preparedness

AES128 → AES CGM

Hash vs. Matrix

NIST Competitions

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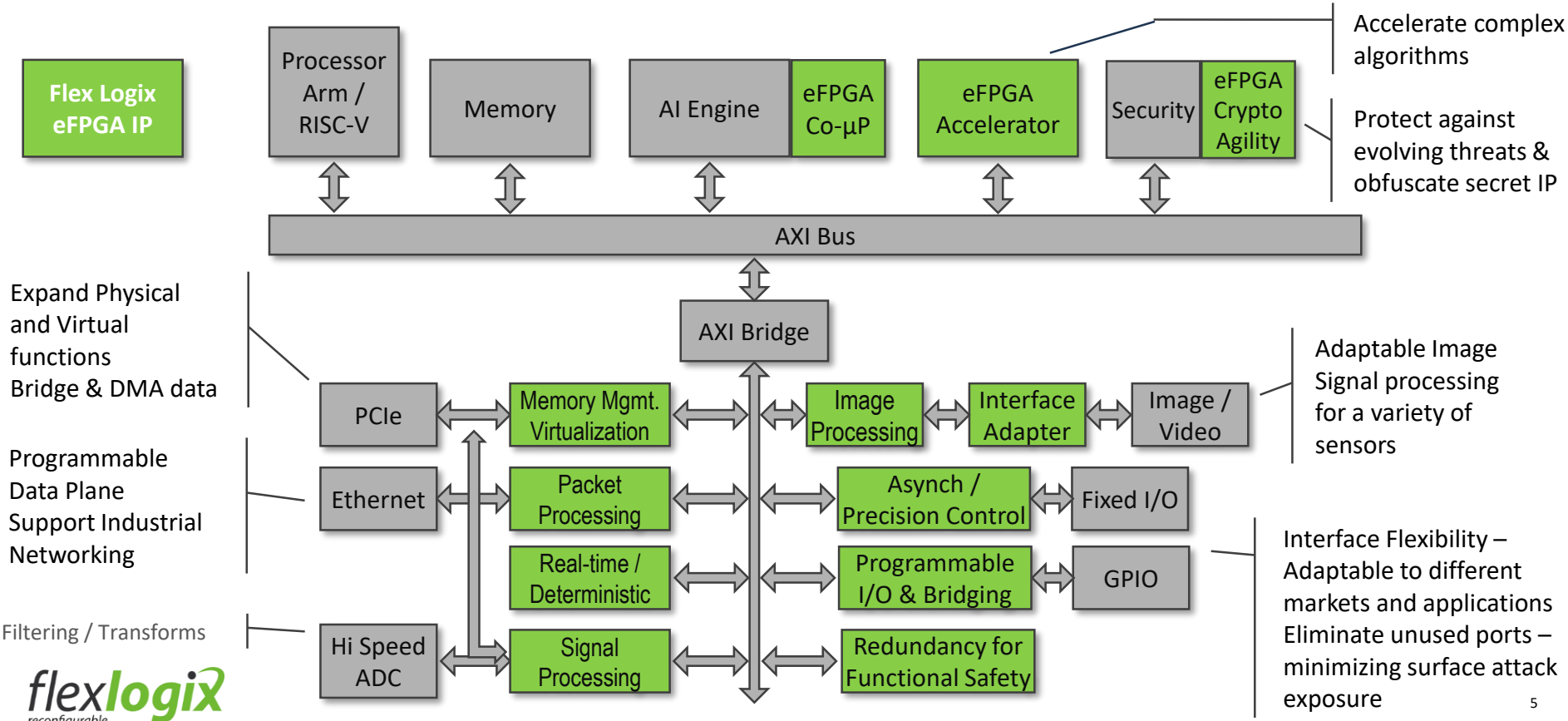
Embedded FPGA Has Many Use Cases



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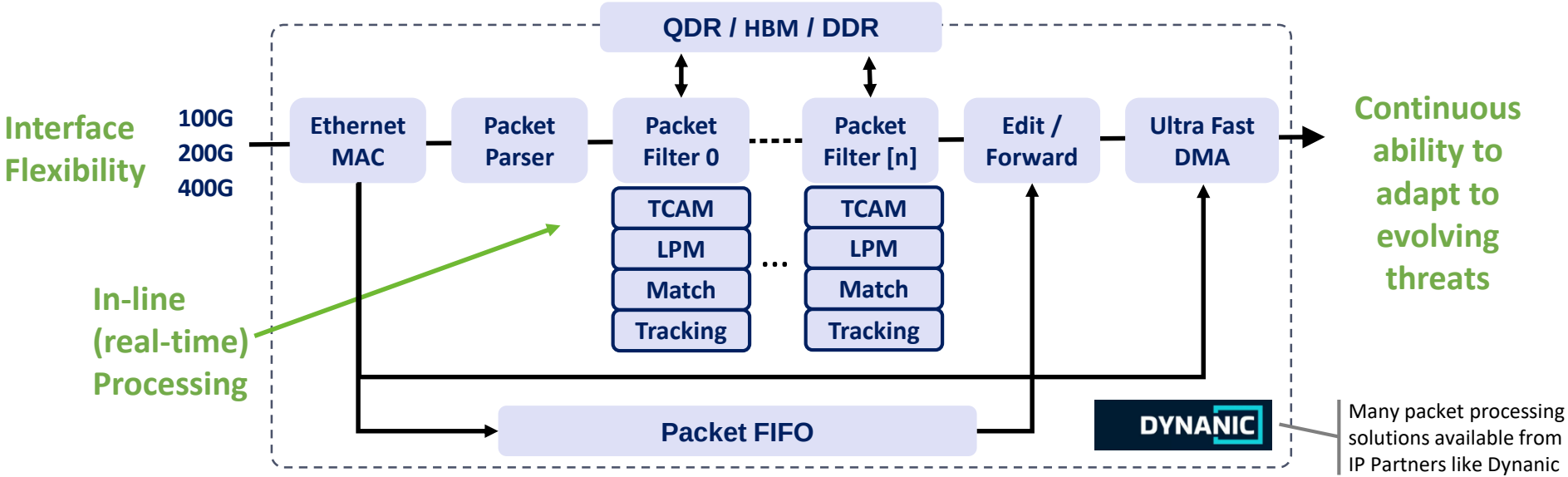
Programmable Data Planes Enable SmartNIC Security

Servers mitigate many malicious attacks, such as Distributed Denial of Service, which require immediate detection & response



eFPGA is the perfect solution for SmartNICs and adaptable Packet Processing

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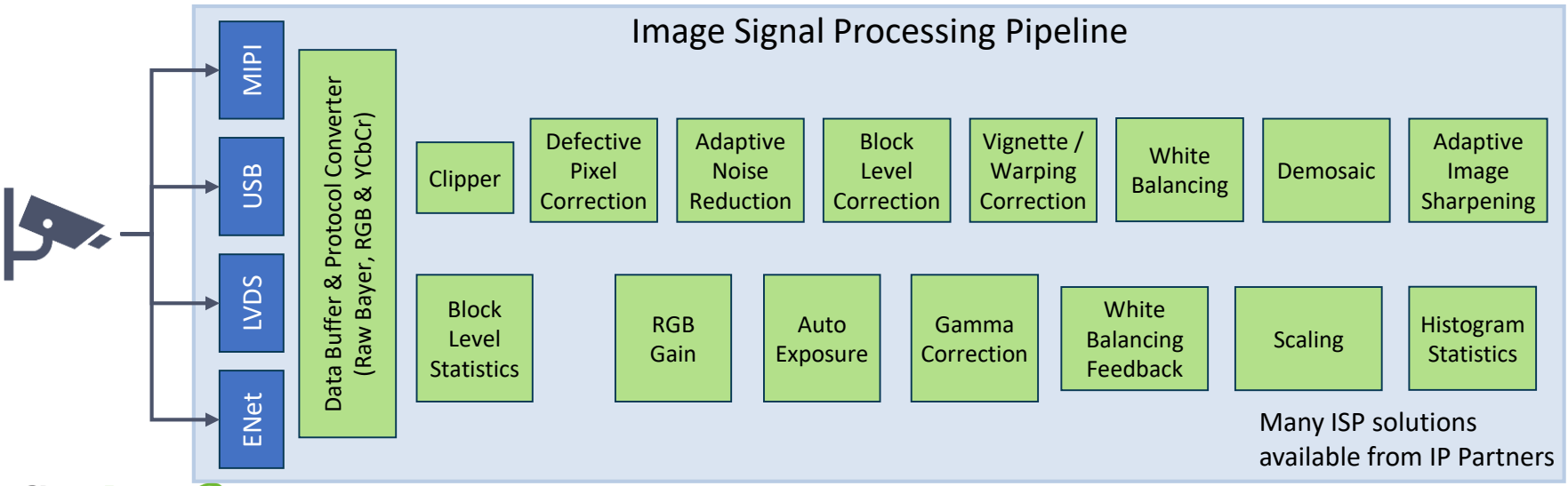
Adaptable Image Signal Processing

Image Signal Processing requirements can be dynamic for each application

Video sources & formats can by vary by sensor	Resolution, frame rate and color depth dependent on application	Parallel pixel processing as well as multiple video channels



Hard IP

EFLX® eFPGA

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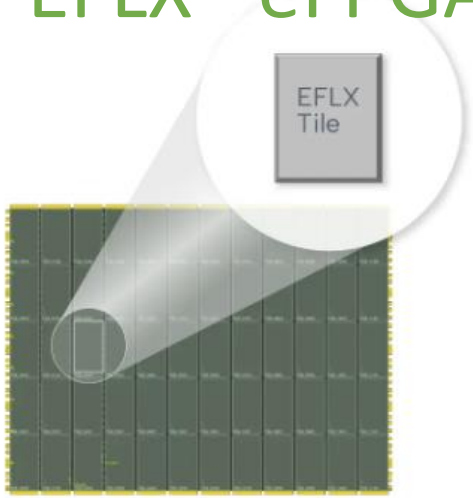
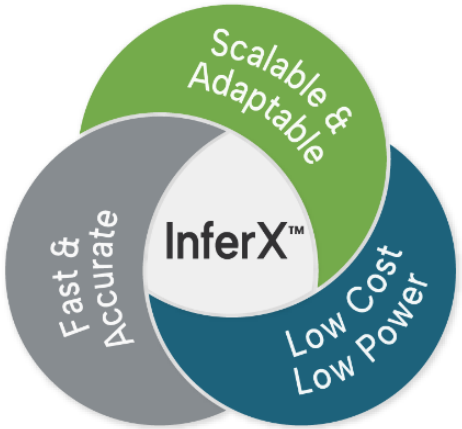
Flex Logix IP Available for Programmable Applications

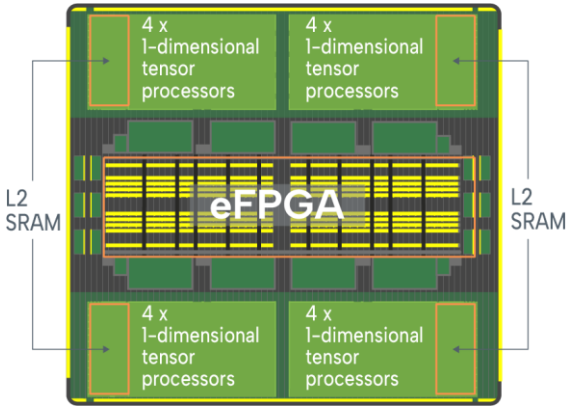
Flex Logix IP available on advanced nodes
TSMC 5nm and INTEL 18A

EFLX® eFPGA





InferX™ DSP & AI



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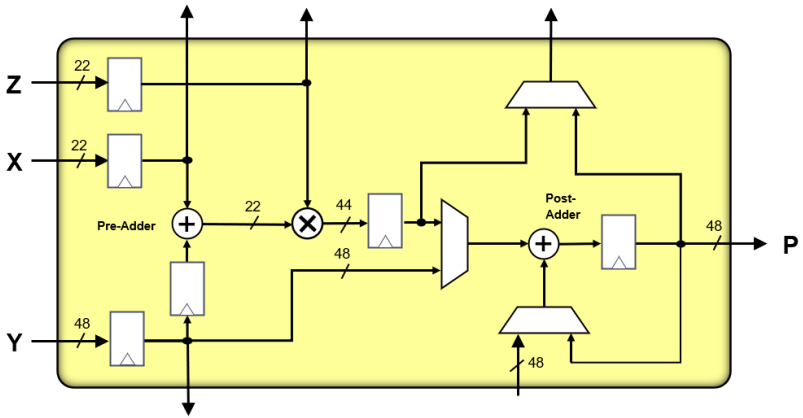
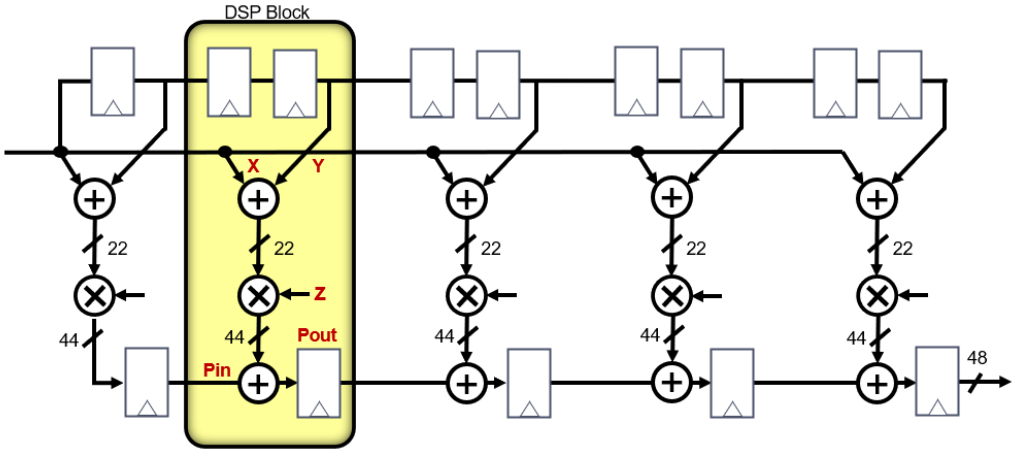
Signal Processing with Flex Logix EFLX DSP

- Flex Logix DSP Blocks → 22x22-bit signed real multiplier with 48-bit accumulator
  - Pre-adder & post-adder can perform 11- and 24-bit complex signed add/sub
  - Built in sign-detection logic and local carry chains for cascading into larger computation

Flex Logix EFLX DSP block



10-tap symmetrical FIR filter using only 5 DSPs



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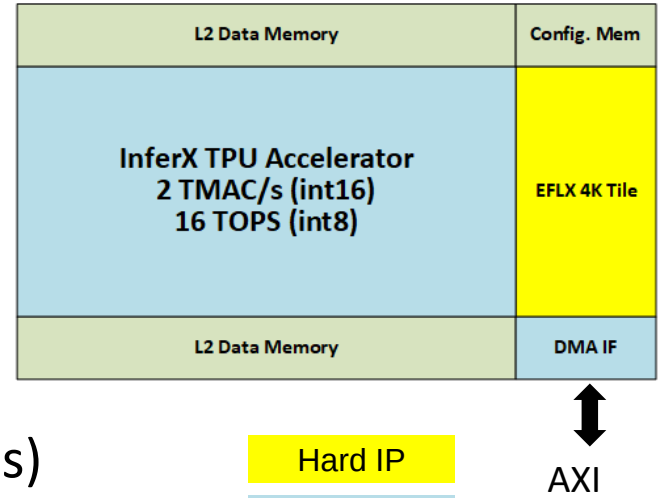
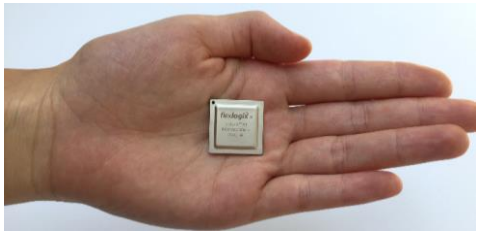
InferX IP World Class DSP+AI Processing at Lowest $/W

- Scalable number of tensor processors
- Tensor processors are configured dynamically
  - optimizes throughput and utilization
  - easy to adapt to new operators + workloads
- INT16 mode for DSP with INT40 accumulation
- INT8 mode for AI (with INT16 and BF16 options)
- High level programming
- Silicon proven





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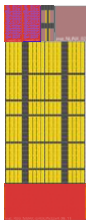
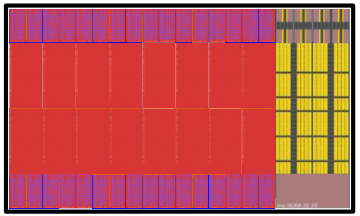
InferX Scalability to Meet a Wide Range of Workloads

Scalable DSP Performance from 1 → 16 → 128 TPUs

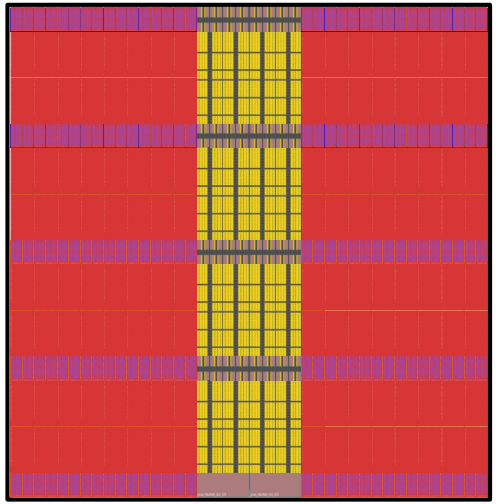
InferX
Tile with 1 TPU
1 TOP



InferX 16 TPU
Tile w/16 TPUs
16 TOPs



InferX 128 TPU
Tile with 128 TPUs / 128 TOPS



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InferX – High Performance, Multi-Operations, Low Latency

DSP

1GHz Operation	µInferX	1 InferX	8 InferX
Complex INT16 1K/2K/4K FFT	500 MS/s (Megasamples/sec)	8.5 GS/s (Gigasamples/sec)	68 GS/s (Gigasamples/sec)
Real INT16x16 FIR 256 taps	0.25 GS/s	4 GS/s	32 GS/s
Real INT16x16 FIR 4096 taps	16 MS/s	0.25 GS/s	2 GS/s
32x32 Complex INT16 Matrix Inversion	10K/sec	0.2M/sec	2.6M/sec
Area (rough est.)	~0.5 mm^2	~3.6 mm^2	~20 mm^2

Vision AI

1GHz Operation	2 µInferX	1 InferX	8 InferX
YOLOv5s (640x640)	32 IPS	260 IPS	1400 IPS
YOLOv5L6 (1280x1280)	2 IPS	16 IPS	130 IPS
DETR 2020 Transformer (1024x1024)	3 IPS	26 IPS	195 IPS
Area (rough est.)	~0.6 mm^2	~2.5 mm^2	~20 mm^2
LPDDR5	1	1	4

Area and performance benchmarks based on TSMC N5/N4 Nodes

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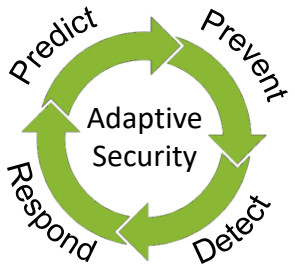
eFPGA Solutions Hold the Key to Security

Cryptography solutions must be agile as decisions made today will be challenged

- Accelerates crypto algorithms w/ parallel processing in eFPGA
- Multiplex cryptography algorithms – Saving die area
- Enhance digital signatures with additive solutions
- Protect “secret” or critical IP with obfuscation
- Mitigate ITAR concerns by adapting to regional requirements



Discrete FPGA Problems	***Flex Logix Solution***		
	Minimize Attack Surface	Algorithm Acceleration	Secure Solutions
Cloning, Overbuilding, Side Channel Attacks, Spoofing, Zero Trust (inc. supply chain), Bitstream Interception/Mutable	Flexible interface capability eliminates unused access ports	Many crypto algorithms can be accelerated in programmable logic RNGs, PUF generation, KDF, ECC	Proven IP solutions from partners Xiphera, Synopsys, CAST

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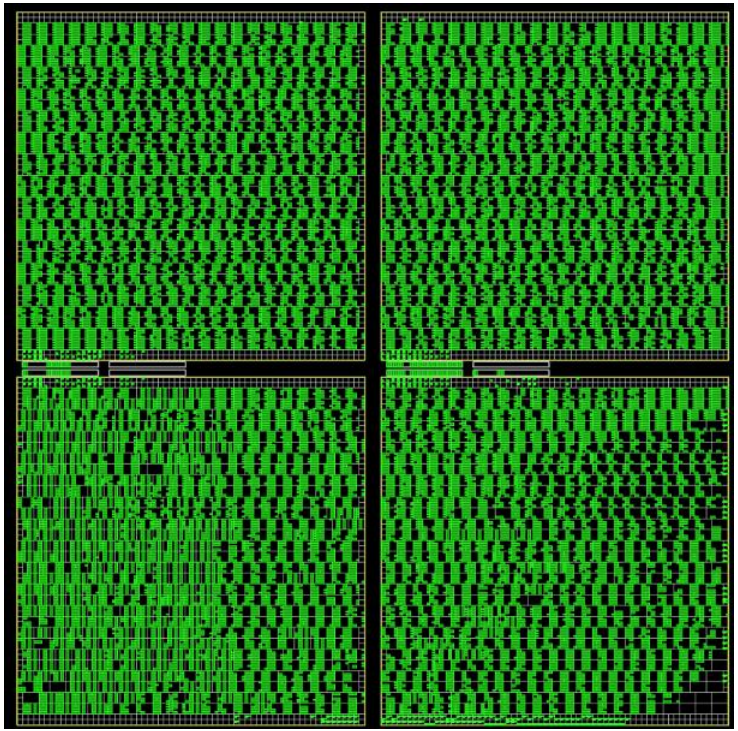
PQC KYBER Encryption Module Flex Logix EFLX IP

ML-KEM Implementation Example

- IP fits compactly into 2x2 EFLX4K Tile Array with > 90% utilization
  - 10K LUTs | 5K Registers | 8 BRAMs
  - Can be implemented on any ASIC or SoC on any technology node
- Fast 225 MHz clock rate @ 64b → 1.8 GB/s
  - Typical, TSMC 7nm



Flex Logix EFLX 4K Tiles

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Secure Critical IP and Algorithms with Obfuscation

Reprogrammable IP in critical interfaces, algorithms and cryptography becomes the keystone to device security & operation

Memory Protection

DMA Isolation | Dynamic Virtual Memory Management | Encryption

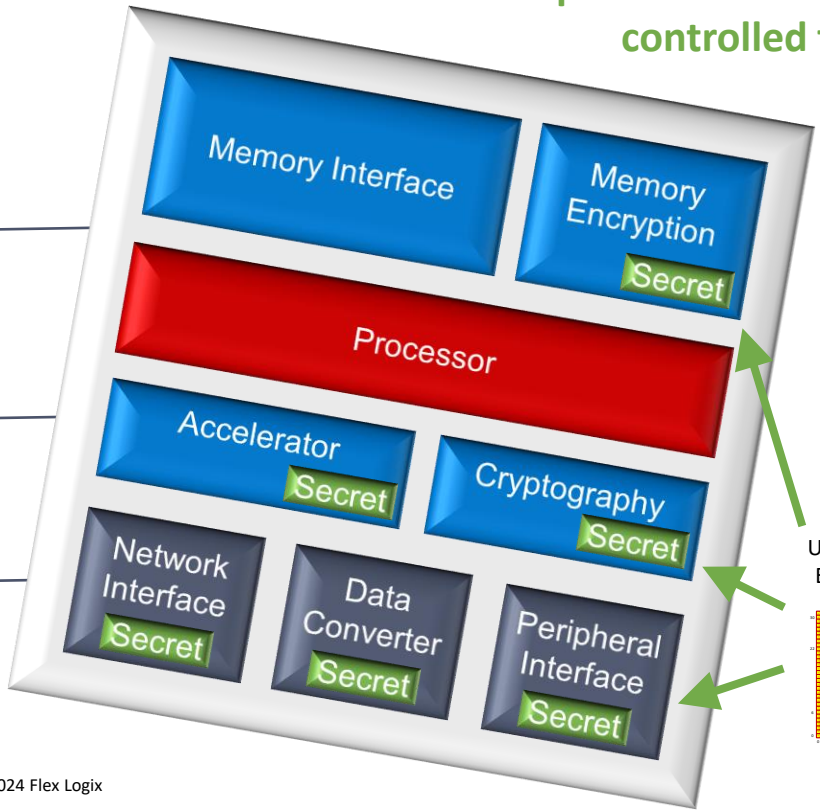
Algorithm Confidentiality

Cryptography | Signal Processing IP | Proxy Re-Encryption | Homomorphic Encryption

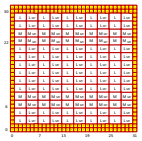
Interface Obscurity

Protocol Processing | Encoding & Decoding | Encryption | Packet Filtering | Authentication (signing)

Add & update secrets at your controlled facility



Ultra Compact EFLX 200 Tile



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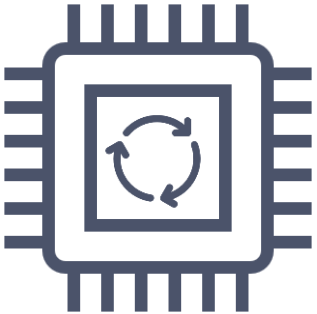
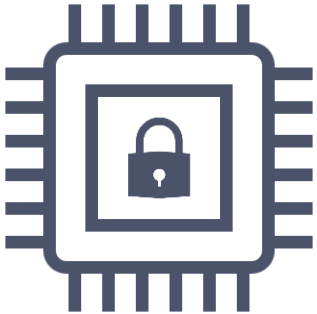
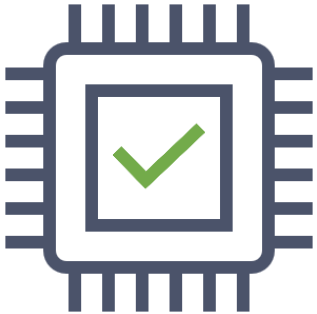
Hybrid Solution = ASIC + FPGA = Best Solution

Solutions today are implemented in either FPGAs or ASICs/SoCs, but Hybrid offers Best of Both

	FPGA	ASIC	HYBRID
			
PROS	Flexible, Adaptable	Highest Performance Lowest Cost & Power	Adaptable Hardware High Performance Low Cost & Power Lowers Design Risk
CONS	High Cost & Power Supply Chain Cloneable/Mutable Side Channel Attacks Hard to Design	Lacks any HW adaptability or flexibility High Design Risk Only SW upgrades	RTL Design Knowledge for highest performance

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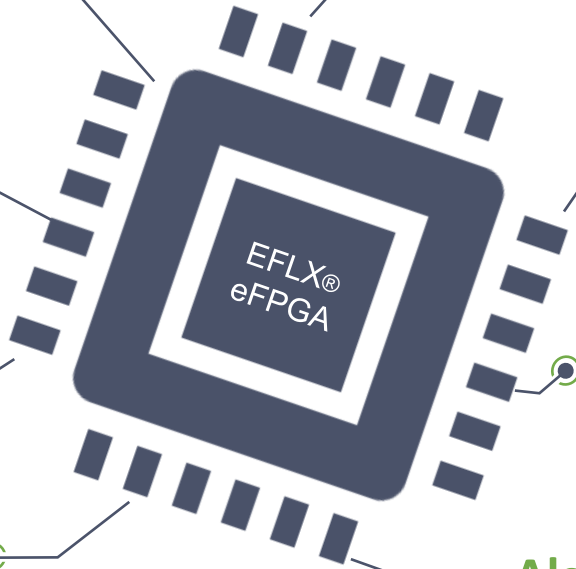
Improve Your ASIC

Save Money
FPGA Integration can reduce mask spins and save engineering cost by moving risky IP to programmable logic

Evolving Protocols
Extend product life by adapting to new interfaces and protocols and supporting changing workloads

Periodic Bug Fixes
Enable updates to fix pesky bugs

Enable Differentiation
Flexibility and adaptability to enable unique features vs competition



Regional Requirements
Meet regional specific protocol and security requirements

Lasting Security
Adapt to evolving security algorithms and threats

Lifecycle Test & Debug
Built in Logic Analyzer w/ run-time debug, bring up analysis , RMA analysis

Algorithm Improvement
Many IP continuously improve such as AI and data plane processing IP

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Summary

Flex Logix eFPGA is the most proven eFPGA Technology on the market

- With over 25 working silicon designs
- Best PPA in the industry
- Best EDA tool chain with Synplify + eXpreso compiler
  - Providing the best design and customer experience
- Proven high-volume deployment with major IC manufacturers
- IP available and proven in more fab nodes than any other supplier
  - TSMC and Intel IP Alliance Partners
- Silicon proven solutions for packet processing, security and SW acceleration

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Learn More and Next Steps

- See us at booth #310 to see demos in action
- Visit Flex Logix Website @ https://flex-logix.com
- Contact our Sales team: info@flex-logix.com

- Test drive your IP with EFLX Compiler
  - Set up a Tools Demo
    - A free 45-day eval system is available for your use after the demo session
    - Get Performance, Power and Area estimates

See for yourself why Flex Logix is #1 for PPA

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